Notice of Allowability	Application No.	Applicant(s)	
	09/943,968	FORBES, LEONARD	
	Examiner	Art Unit	
	Dac V. Ha	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 02/28/05*.

2. ☒ The allowed claim(s) is/are *1-48*.

3. ☒ The drawings filed on *02/28/05 and 01/31/02* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dac V. Ha
Primary Examiner
Art Unit: 2634

Allowable Subject Matter

1. Claims 1-48 are allowed.

2. The following is a statement of reasons for the indication of allowable subject matter:

The present invention relates to simultaneous transmission of digital data and clock signals to eliminate skewing of the data and clock signals with respect to each others. Upon further consideration, prior art of record, taking individually or collectively, fails to fairly teach such method and apparatus including "a phase shift keying circuit for performing phase shift keying of said digital signal onto said clock signal to create a lead output signal and a lag output signal; a digital signal demodulator for demodulating said lead output signal and said lag output signal from said phase shift keying circuit to retrieve said digital signal; and a clock signal demodulator for demodulating said lead output signal and said lag output signal in conjunction with said digital signal to retrieve said clock signal" in independent claim 1; "a lead phase shift network receiving said sinusoidal oscillator signal and said digital signal for producing a positive phase shift in a lead output signal when said digital signal has a logical high value; and a lag phase shift network receiving said sinusoidal oscillator signal and a complementary digital signal for producing a negative phase shift in a lag output signal when said complementary digital signal has a logical high value" in independent claim 24; "a differential amplifier for comparing said lead signal and said lag signal to produce a differential output signal; a transistor amplifier circuit for receiving said differential output signal and producing a transistor signal dependent upon the square of an AC

component of said differential output signal; an RC low pass filter for receiving said transistor signal and outputting a voltage signal; a voltage comparing circuit for receiving said voltage signal and a voltage reference signal to produce a demodulated digital data signal" in independent claim 32; and "generating a sinusoidal oscillator signal, a digital signal and a complementary digital signal; creating a lead output signal from said sinusoidal oscillator signal and said digital signal; creating a lag output signal from said sinusoidal oscillator signal and said complementary digital signal; transmitting said lead output signal and said lag output signal on matched interconnection lines to a vicinity of a clocked element; demodulating said lead output signal and said lag output signal for retrieving said digital signal; demodulating said lead output signal and said lag output signal using said digital signal for retrieving a clock signal; and inputting said digital signal and said clock signal into said clocked element" in independent claim 38 (claims 2-23, 25-31, 33-37, 39-48 depend therefrom). Thus, claims 1-48 are found to be novel and unobvious over prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dac V. Ha
Primary Examiner
Art Unit 2634